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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,707	HORANZY ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,13-15,17,18,20,24-31,33,37-42 and 44* is/are rejected.

7)☒ Claim(s) *7,9-12,16,19,21-23,32,34-36,43 and 45-47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claims 32, 43, and 47 are objected to because of the following informalities:

Re claims 32 and 43, the phrase "shared memory" does not include the word "volatile".

Re claim 47, the phrase "static random access memory" does not include the phrase "dual port".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 38 and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 38 recites the limitation "the second processor" in line 2. There is insufficient antecedent basis for this limitation in the claim in that no second processor has previously been recited in claim 38 or claim 37 from which claim 38 depends.

Claim 41 depends from claim 38 and likewise is indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 5, 6, 8, 13-15, 17, 18, 20, 24-27, 30, 31, 33, 37, 38, 40-42, 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reuter in view of Von Ahnen.

Re claims 1 and 37, Reuter discloses a method and mechanism for bootstrapping a processor from a volatile memory device connected to the processor, comprising the steps of:

asserting reset lines of the second processor (column 5, lines 42-45);

loading boot code (column 2, lines 11-16) for the second processor into the volatile memory device (column 3, lines 55-59); and

de-asserting the reset lines of the second processor (column 6, lines 6-10), wherein the processor performs the bootstrap procedure using the boot code stored in the volatile memory device (column 4, lines 17-26).

Reuter fails to disclose bootstrapping the first processor from a flash device and loading the boot code from the flash device.

Von Ahnen teaches booting primary processor from a ROM associated with the primary processor (column 5, lines 50-52, FIG. 2) after which an application program is loaded into the RAM of a secondary processor (column 5, lines 52-55, lines 59 and 60, FIG. 2). Von Ahnen does not specifically address booting from a flash device. The examiner takes official notice that a flash device functions as read-only memory (ROM) after the programming of the flash device was completed and the actual boot process is only possible at that time. ROM memories are implemented differently including the use of flash devices, EPROMs, EEPROMs, etc. In Von Ahnen, after the loading the application program to both RAM's (for the primary and secondary processor), the primary and secondary processors begin processing data traffic (column 5, lines 62-64). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the initialization method and application program transfer, as suggested by Von Ahnen for the method and mechanism disclosed by Reuter in order to bootstrap the processor from a flash device and load the boot code for the second processor from a flash device.

Re claims 2 and 38, Reuter further discloses the method and mechanism, wherein the memory control signals of the second processor and the hardware handshake signals of the volatile memory device are combined to imitate a boot from a flash device (column 4, lines 31-37, lines 61-67, column 5, lines 1-5).

Re claims 5 and 41, Von Ahnen further teaches a complex programmable logic device comprises logic units to correctly combine the memory control signals of the

second processor and the hardware handshake signals of the volatile memory (column 6, lines 56 and 57, FIG. 2).

Re claims 6 and 42, Von Ahnen further teaches the method and mechanism, wherein a plurality of processors (column 5, lines 23-26) are bootstrapped by loading the boot code for the plurality of processors into a plurality of volatile memory devices, wherein each processor is connected to a different volatile memory (FIG. 2).

Re claims 8 and 44, Reuter further discloses the method and mechanism, wherein the volatile memory device is a static random access memory (column 3, lines 55 and 56).

Re claim 40, Reuter further discloses the method, wherein the reset lines are controlled by the master processor (column 3, lines 47-54).

Re claim 13, Von Ahnen further teaches a system for bootstrapping a processor from a volatile memory device (FIG. 2), comprising:

a second processor with associated flash device (FIG. 2);

a logic device for generating reset lines of the second processor and de-asserting the reset lines based on a control signals from the first processor (column 6, lines 56 and 57, FIG. 2);

the volatile memory device for storing boot code for the second microprocessor loaded from the flash device after the first processor has been bootstrapped (column 5, lines 50-55, lines 59 and 60, FIG. 2); and

the processor connected to the volatile memory device connected to the volatile memory device, wherein when the reset lines of the second processor are de-asserted,

the second processor bootstraps from the boot code stored in the volatile memory device (column 5, lines 59 and 60, lines 62-64, FIG. 2).

Re claim 14, Reuter further discloses the system, wherein the boot code of the processor and hardware handshake signals of the volatile memory device are combined to imitate a boot from a flash device (column 4, lines 31-37, lines 61-67, column 5, lines 1-5).

Re claim 15, Von Ahnen further teaches the system, wherein the logic unit is a complex programmable logic device (FIG. 2).

Re claim 17, Von Ahnen further teaches the complex programmable logic device comprises logic units to correctly combine the memory control signals of the processor and the hardware handshake signals of the volatile memory (column 6, lines 56 and 57, FIG. 2).

Re claim 24, Von Ahnen further teaches the system, further comprising a flash device connected to the second processor (FIG. 2) having boot code for the processor, wherein the first processor determines whether to bootstrap the second processor using the boot code in the flash device connected to the second processor or the boot code in the volatile memory device (column 6, lines 27-36) based on a user selection (Von Ahnen further teaches initiating boot from either ROM or RAM associated with the secondary processor upon receipt of an interrupt at any time during routine operation and thus implementing user selectable boot generating an interrupt signal – column 6, lines 45-50).

Re claim 25, Von Ahnen further teaches the first processor sets a command register in the logic device to configure logic units for the selected bootstrap procedure (column 6, lines 51-55).

Re claim 26, Von Ahnen further teaches a method for bootstrapping a processor from either a flash device or a volatile memory, comprising the steps of:

bootstrapping a master processor (column 5, lines 50-52);

determining whether a flash bootstrap procedure or a volatile memory device bootstrap procedure has been selected for the second processor (column 6, lines 27-36);

setting a command register in logic device to configure logic units for the selected bootstrap procedure (column 6, lines 51-55);

if the flash bootstrap procedure was selected:

performing bootstrap procedure from the flash device associated with the second processor (column 6, lines 37-40);

if the volatile memory bootstrap procedure was selected:

asserting reset lines of the processor (column 6, lines 40-44);

loading boot code for the second processor from a flash device associated with the first processor into the volatile memory (column 5, lines 50-55, lines 59 and 60, FIG. 2); and

de-asserting the reset lines of the processor, wherein the processor bootstraps from the boot code stored in the volatile memory device (Von Ahnen further teaches booting to system mode and execution of an application program after the application

program has been stored in the second processor's RAM and thus teaches de-asserting the reset lines for the second processor prior of program execution – column 6, lines 40-44, column 5, lines 52-55, lines 59 and 60, lines 62-64).

Re claim 27, Reuter further discloses the method, wherein the memory control signals of the second processor and the hardware handshake signals of the volatile memory device are combined to imitate a boot from a flash device (column 4, lines 31-37, lines 61-67, column 5, lines 1-5).

Re claim 30, Von Ahnen further teaches the method, wherein a complex programmable logic device comprises logic units to correctly combine the memory control signals of the processor and the hardware handshake signals of the volatile memory (column 6, lines 56 and 57, FIG. 2).

Re claims 18 and 31, Von Ahnen further teaches the system and method as per claims 13 and 26, wherein the a plurality of processors are bootstrapped (column 5, lines 23-26) by loading the boot code for the plurality of processors into a plurality of volatile memory device, wherein each processor is connected to a different volatile memory (FIG. 2);

Re claims 20 and 33, Reuter further discloses the system and method, wherein the volatile memory device is static random access memory (column 3, lines 55 and 56).

Claims 3, 4, 28, 29, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reuter in view of Von Ahnen, and further in view of Klein.

Re claims 3 and 39, Reuter and Von Ahnen disclose the method and mechanism as per claims 1 and 38.

Reuter and Von Ahnen fail to disclose a complex programmable logic device generating the reset lines of the processor.

Klein teaches a ROM shadowing circuit (RSC) (column 3, line 55) used for generating a reset signal to a processor during ROM shadowing operation (column 4, line 67, column 5, lines 1-7). In Klein, the RSC is used for copying firmware routines from the ROM to the RAM during computer system initialization (column 3, lines 55-57). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the RSC, as suggested by Klein for the method and mechanism disclosed by Reuter and Von Ahnen in order to reset the processor's lines with a complex programmable logic device.

Re claim 4, Klein further teaches the method, wherein the reset lines are controlled by the first processor and handled by the complex programmable logic device (column 5, lines 7-13, FIG. 3).

Re claim 28, Klein further teaches the method, wherein a complex programmable logic device generates the reset lines of the second processor (column 5, lines 7-13, FIG. 3).

Re claim 29, Klein further teaches the reset lines controlled by the master processor (column 5, lines 7-13, FIG. 3).

Allowable Subject Matter

Claims 38 and 41 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 7, 9-12, 16, 19, 21-23, 32, 34-36, 43, and 45-47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claims 7, 19, 32, and 43, the prior art fails disclose or suggest the claimed method, wherein "the first processor provides identity to each of the plurality of processors by posting information through volatile memory".

Re claims 9, 21, 34, and 45, the prior art fails disclose or suggest the claimed method implemented with "dual port random aces memory".

Re claims 10, 22, 35, and 46, the prior art fails disclose or suggest "synchronous static random access memory".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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